Rejection Under 35 U.S.C. 103(a)

Claims 1-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sanada (US 5,843,527) in view of Morimoto (US 5,898,588) and Venkatesh et al. (US 6,074,443).

According to the Office action:

> Sanada has the basic processing apparatus.
>
> Morimoto teaches interrupting the wafer manufacturing process if there is a delay or error in one of the processing station[s].
>
> Venkatesh et al. teaches optimizing the control of the wafer manufacturing processing apparatus by sending the wafer into another available station if there is a delay or error in a station.
>
> One of ordinary skill in the art would use the software instruction and hardware instruction to control the process of Sanada in order to increase throughput and control malfunctions in all stages of the operation.

The rejection is traversed.

It is respectfully submitted that the Office action fails to present a *prima facie* case of obviousness of the specific subject matter of Applicants' claims. The cited combination of references fails to teach or suggest the specific features of Applicants' claims. Furthermore, the Office action fails to support *prima facie* obviousness of the claims, because, e.g., the rejection does not specifically identify the differences between Applicants' claims and the cited references, and fails to explain how or where the specifically recited features of Applicants' independent and dependent claims are suggested in the cited prior art.

The Office action's conclusion of obviousness is not supported by the cited references. Contrary to the rejection, one of ordinary skill "using the software instruction and hardware instruction [of Morimoto or Venkatesh et al.] to control the process of Sanada" would not have arrived at the claimed invention. As detailed below, nothing in

the combination of references would have taught or suggested the details of Applicants' invention as claimed. It is therefore requested that the present rejections be withdrawn.

The Claims Relate to Spin-Coating

Certain of Applicants' pending claims relate to process control systems (and related apparatus and methods) useful for carrying out steps that make up spin-coating processes, i.e., processes that apply a process solution to a substrate and then spin the substrate to distribute the process solution over the substrate surface. The steps may be conventional steps such as applying a process solution to a substrate (e.g., a beginning or ending of application of a process solution to a substrate); a substrate movement such as a start, a stop, or an acceleration or deceleration of rotation of a substrate; or movement of another component such as a dispense arm; etc.

The present claims relate to how one or a series of steps of a spin-coating process can be precisely controlled and performed, e.g., to process control and control of timing of one step of a spin-coating process with respect to the timing of another step of the spin-coating process. For example, according to certain claims, one or more steps of a spin-coating process are not controlled by conventional, e.g., serial or other round-robin process control algorithms, which produce timing inaccuracy and accumulation of timing variability, for example based on the time taken to execute intervening subroutines before performing a next step in a sequence (e.g., inaccuracy caused by subroutines following an end of dispense). (See, e.g., Applicants' original description at page 4, line 1 through page 6, line 18.)

The outstanding Office action fails to specifically describe how or where the cited references are believed to teach or to suggest the specific features of Applicants' claims. Specifically not mentioned by the Office action are features of methods of spin-coating process solutions onto substrates, and related apparatus, that include:

- "interrupted control" during a spin-coating process, wherein serial (e.g., "round-robin") control of a spin-coating process is interrupted to execute a process command

- the use of interrupt service routines in a spin-coating method

- hardware or software interrupt signals used in a spin-coating method as claimed, or

- parallel timers used to control a spin-coating process by measuring multiple durations in parallel, for initiating multiple different subsequent spin-coating processing steps at a time following one or more earlier spin-coating processing steps.

The Cited References

Sanada

The Office action states that Sanada describes a basic processing apparatus.

The Sanada reference describes "methods of applying a coating solution to spinning substrates." (See, e.g., the Sanada Abstract.) In other words, Sanada relates to individual substrate processing units, i.e., spin-coating apparatus, used to process (spin-coat) a substrate (e.g., wafer) or a series of wafers. Sanada identifies as an object of the invention: "to provide a coating solution applying method and apparatus incorporating improved rotational frequency controls to drastically reduce the quantity of coating solution supplied to form a coating film." (See Sanada at column 3, lines 1-7.) The Sanada reference specifically relates to the use of different rotational frequencies in supplying a coating solution, and forming a film. (See Sanada at column 3, lines 8 through 35.)

The Sanada reference is not asserted to show or suggest, by itself, the subject matter of Applicants' pending claims. Accordingly, Sanada is not by itself considered to teach or suggest the claimed coating methods, including the control of spin-coating processes using, e.g., interrupted serial control processes; interrupt service routines; hardware or software interrupt signals; or parallel timers.

Instead, the Office action relies on secondary references, Morimoto and Venkatesh et al., in asserting rejections based on the combined teachings of these three references. The secondary references are asserted to make up for the shortcomings of the primary Sanada reference, i.e., the lack of a teaching or suggestion of the claimed invention by the primary reference.

Morimoto

The Morimoto reference fails to make up for the shortcomings of the Sanada reference. For example, the Morimoto reference fails to specifically teach or suggest features of Applicants' claims, such as spin-coating processes that include the following features:

- "interrupted control" during a spin-coating process, wherein serial (e.g., "round-robin") control of a spin-coating process is interrupted to execute a separate process command within the spin-coating process
- the use of interrupt service routines in a spin-coating method
- hardware or software interrupt signals used in a spin-coating method as claimed, or
- parallel timers used to control a spin-coating process by measuring durations for initiating multiple different subsequent spin-coating processing steps at a time following one or more earlier spin-coating processing steps.

According to the Office action, Morimoto teaches "interrupting the wafer manufacturing process if there is a delay or error in one of the processing stations." Even if this is taken as true, the overall Morimoto reference still does not teach or suggest the specific features of Applicants' claims.

While the two cited references, Sanada and Morimoto, both relate to aspects of semiconductor processing, the references at the same time relate to different aspects of semiconductor processing methods and apparatuses.

The Sanada reference relates to steps and controls used with an individual spin-coating processing station, as they relate to coating a single substrate (e.g., silicone wafer). In other words, Sanada relates to an individual substrate-processing unit that is used to process (spin-coat) a substrate (e.g., wafer) or a series of wafers.

Morimoto, on the other hand, relates more generally to the steps and controls of multiple-coating station processing apparatuses and methods, as they relate to the controlled movement of multiple substrates between the multiple coating stations. For example, Morimoto describes "[a] method and apparatus for successively conveying substrates between a plurality of processing units." (See, e.g., the Morimoto Abstract.) Also:

> the [Morimoto] invention is directed to a method of controlling a substrate processing apparatus which successive [sic] causes the successive conveyance of substrates to a plurality of processing units via a preset transport path and causes the processing of the substrates thus conveyed.

Morimoto, at column 1, lines 61-66.

The Morimoto reference emphasizes methods of controlling movement of substrates between multiple processing units. To the extent that Morimoto describes "suspension" of control, that "suspension" relates to "suspending" conveyance of substrates from one station to the next. E.g.:

> The method comprises the step of: executing a control sequence in a skip mode when one of the plurality of processing units causes an alarm to be raised which indicates the occurrence of an abnormality. Control in the skip mode continues and completes the processing and conveyance of each substrate already on the transport path of the processing units located in and after the processing unit for which an alarm has been raised and suspends the conveyance of each substrate in the transport path of the processing units located before the processing unit for which the alarm has been raised.

The Morimoto patent at column 1, line 66 through column 2, line 9.

The Morimoto reference generally relates to movement of substrates between multiple substrate processing units. The reference lacks a specific description of a spin-coating process, as claimed, e.g., including the features of interrupted serial control, parallel timers, interrupt service routines, etc.

Venkatesh et al.

The Venkatesh et al. reference fails to overcome the shortcomings of the Sanada reference combined with Morimoto.

The combination of Venkatesh et al., with Sanada (and Morimoto), is also insufficient in supporting a teaching or suggestion of specific subject matter of the present claims.

According to the Office action, Venkatesh et al. teach "optimizing the control of the wafer manufacturing processing apparatus by sending the wafer into another available station." Even if this were taken as accurate, such a teaching would still fail to teach or suggest the specific features of Applicants' claims, such as the use of interrupted serial process control in a spin-coating process.

While the Venkatesh et al. reference, like Sanada and Morimoto, also relates to an aspect of semiconductor processing, the Venkatesh et al. also relates to steps and controls of multiple-coating station processing apparatuses and methods. According to the Venkatesh et al. Abstract, for example, the invention relates to priority-based scheduling of wafer processing within a multiple chamber semiconductor wafer processing system (cluster tool). "The sequencer assigns priority values to the chambers in a cluster tool, then moves wafers from chamber to chamber in accordance with the assigned priorities." See also column 3, lines 29-36 of the Venkatesh et al. patent.

Distinctly, Sanada, as previously discussed, relates to steps and controls of individual spin-coating processing station (even if within a larger group of processing stations, such as a "cluster"). The Vankatesh et al. reference does not combine with Sanada to produce a unified teaching of the claimed invention, relating to controlling spin-coating methods. For example, the cited combination of references still fails to teach or suggest Applicants' claimed spin-coating coating methods, including control of spin-coating processes using, e.g., interrupted serial control processes; interrupt service routines; hardware or software interrupt signals; or parallel timers.

Specific Claim Features

The Office action summarily concludes that one of skill would

> use the software instruction and hardware instruction to control the process of Sanada in order to increase throughput and control malfunctions in all stages of the operation.

This basis of rejection fails to address specific features of Applicants' claims, and how or where they are found in the prior art.

Moreover, as described *supra*, the secondary references do not relate specifically to spin-coating processes. They fail to teach specific features of Applicants' claimed subject matter. Even generally, their teachings, which relate to broader semiconductor processing and substrate-transport, are not necessarily directly applicable or transferable to the context of specific spin-coating processes.

Considering this, the above basis of rejection is tantamount to rejecting claims on grounds that *any use of software or hardware instruction intended to increase throughput and control of a spin-coating operations, would have been obvious*. Without a specific showing that a cited prior art reference either teaches or suggests all features of Applicants' spin-coating inventions, the rejections based on obviousness are legally unsupported and should be withdrawn.

A requirement for establishing *prima facie* obviousness is that the prior art must teach or suggest all features of a claim. How the features are taught or suggested in the prior art should also be explained in making a rejection.

The Office action, with its blanket conclusion of obviousness of all of Applicants' pending claims, fails to identify how the combined references teach or suggest the specific features of Applicants' claims. As such, this summary rejection of all of Applicants' claims should be withdrawn.

Specific features of Applicants' claims that are not addressed by the Office action, include the following.

Claims 1-8

Claim 1 recites a method for controlling a process of spin-coating a developer solution onto a substrate. The method includes the feature of interrupting serial process control of the spin-coating process, with an interrupt signal, to execute a process command. Generally, such systems are described in Applicants' specification, e.g., at page 21, line 31 through 22, line 2, and include spin-coating processes wherein serial

control is interrupted by an interrupt signal, whereupon the process control system executes a pre-programmed process command and then returns to serial control.

As indicated by the rejection, these features of a spin-coating process are neither taught nor suggested by the Sanada reference.

These features are also not found in the Morimoto reference. The Morimoto reference describes transfer of substrates between multiple processing stations, one or more of which may be a spin coater (see, e.g., column 5, line 52) wherein conveyance of substrates from one station to the next may be "*suspended.*" I.e., upon occurrence of an alarm at a particular processing unit within the series of processing units, Morimoto describes suspension of "conveyance of each substrate in the transport path of the [multiple] processing units located before the processing unit for which the alarm has been raised." See the Morimoto reference, e.g., at column 2, lines 5-9.

The Morimoto reference fails to specifically teach or suggest methods involving interrupting serial process control of a spin-coating process, with an interrupt signal to execute a process command, as featured in Applicants' claim 1. The "suspension" of Morimoto refers to suspending conveyance of substrates, not to interrupting serial control of the steps of the spin-coating process as described and claimed by Applicants.

The Venkatesh et al. reference likewise fails to teach or suggest interruption of a spin coating process followed by execution of a spin-coating process command. The rejection of claim 1, therefore, on the stated grounds, should be withdrawn.

The rejections of dependent claims 2 through 8 should be withdrawn for reasons stated with respect to claim 1, upon which claims 2 through 8 depend. Additionally, dependent claims 2 through 8 recite additional features that are neither taught nor suggested by the cited combination of reference. These include, e.g., the features of: an interrupt service routine; the use of multiple timers to measure different durations; the use of software and hardware interrupt signals, optionally upon the occurrence of start or end of a solution dispense; and process commands selected from turntable or dispenser movement. The Office action fails to address these features of Applicants' claims, and the rejections should be withdrawn.

Claim 9

Claim 9 recites a feature of interrupted serial process control to spin-coat both photoresist solution and developer solution. Such a process is neither described by nor suggested by the Sanada reference, or by the Sanada reference in combination with Moritomo and Venkatesh et al. Also, the rejection of these specific features is not explained by the general grounds of rejection of Office action -- the Office action fails to specify how or where these features are found in or suggested by the cited prior art references, or how one of skill would have been motivated to arrive at the claimed features of a spin-coating process. This rejection should be withdrawn.

Claims 10-20

Claim 10 recites a feature of a spin-coating method that includes executing process commands at durations measured "in parallel" from a process event. This claimed method is neither taught nor suggested by the cited combination of references. Also, the rejection of these features is not explained within the Office action.

Dependent claims 11 through 20 recite additionally distinct features including: specifically measuring two or more durations from a single process event; control to within 5 or 1 millisecond; the use of a hardware interrupt, e.g., to identify a selected process event such as a beginning or end of dispenser movement, a beginning of solution dispense; control of a process command selected from a start or end of dispense or turntable acceleration or deceleration.

Claim 21

Claim 21 recites features of a hardware interrupt being sent to a process control system upon a trigger event, execution of an interrupt service routine, and two or more timers in parallel. These features are not identically described or otherwise suggested by the combination of references. The Office action fails to explain how or where these features are believed to be taught by or suggested by the cited references.

Claims 22-26

Claim 22 recites the feature of interrupted serial process control, which is not identically described or otherwise suggested by the cited combination of references. Dependent claims 23 through 26 recite additional features such as an interrupt service routine and multiple timers, which are further patentable over and neither taught nor suggested by the cited combination of references. The Office action fails to explain how or where these features are believed to be taught by or suggested by the cited references.

Claim 27

Claim 27 recites the features of two or more durations measured in parallel from one or more earlier process events, following which are executed two or more process commands. These features are neither taught nor suggested by the cited combination of references. The Office action fails to explain how or where these features are believed to be taught by or suggested by the cited references.

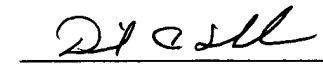
Claim 28, 29, and 30

Claims 28, 29, and 30 recite spin coating equipment that includes features as recited in method claims discussed above. These features are neither taught nor suggested by the cited references. The Office action fails to explain how or where these features are believed to be taught by or suggested by the cited references.

In conclusion, for reasons stated above, the rejections of Applicants' pending claim, based on the cited prior art references, are not supported by the cited references. It is respectfully requested that the pending claims be reconsidered. Early and favorable reconsideration and allowance are respectfully requested.

The Examiner is invited to contact the undersigned, at the Examiner's convenience, should the Examiner have any questions regarding this communication or the present patent application.

Respectfully Submitted,

By: 

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